WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit, comprising:

a first terminal receiving an external power supply voltage provided from outside;

a voltage generating circuit lowering said external power supply voltage and generating an internal voltage;

an internal circuit using said internal voltage;

an A/D conversion circuit converting said internal voltage from an analog value to a digital value so as to output a digital signal to the outside; and

a second terminal providing said digital signal to the outside.

2. The semiconductor integrated circuit according to claim 1, wherein

said internal voltage is an operation power supply voltage of said internal circuit, and

said voltage generating circuit includes

a reference voltage generating circuit generating a reference voltage of said operation power supply voltage,

a differential amplifying circuit receiving said operation power supply voltage and said reference voltage at complementary two inputs, and

a voltage conversion circuit converting said external power supply voltage in response to an output of said differential amplifying circuit so as to output said operation power supply voltage.

3. The semiconductor integrated circuit according to claim 1, wherein

said internal voltage is a reference voltage serving as a reference of an operation power supply voltage of said internal circuit, and

said voltage generating circuit includes

a reference voltage generating circuit generating said reference voltage,

a differential amplifying circuit receiving said operation power supply voltage and said reference voltage at complementary two inputs, and

a voltage conversion circuit converting said external power supply voltage in response to an output of said differential amplifying circuit so as to output said operation power supply voltage.

4. The semiconductor integrated circuit according to claim 1, further comprising:

a third terminal for input of an analog voltage; and

a selector selecting and providing one of said internal voltage and said analog voltage to said A/D conversion circuit.

5. The semiconductor integrated circuit according to claim 1, wherein

said internal voltage is an operation power supply voltage of said internal circuit,

said voltage generating circuit includes

a reference voltage generating circuit generating a reference voltage,

a differential amplifying circuit receiving said operation power supply voltage and said reference voltage at complementary two inputs, and

a voltage conversion circuit converting said external power supply voltage in response to an output of said differential amplifying circuit so as to output said operation power supply voltage,

said A/D conversion circuit receives said operation power supply voltage and said reference voltage at first and second input nodes respectively, and converts said operation power supply voltage and said reference voltage to first and second digital values respectively,

said internal circuit includes

first and second registers temporarily holding said first and second digital values respectively,

an operation circuit outputting a difference between said first and second digital values held in said first and second registers respectively as a third digital value, and

a third register temporarily holding said third digital value, and

the values held in said first to third registers are output from said second terminal.

6. The semiconductor integrated circuit according to claim 5, wherein

said voltage generating circuit further includes a fourth register, and

said reference voltage generating circuit regulates said reference voltage in accordance with a value held in said fourth register.

7. The semiconductor integrated circuit according to claim 5, wherein

said voltage generating circuit further includes a fourth register, and

said voltage conversion circuit adjusts drivability to drive a node outputting said internal power supply voltage in accordance with a value held in said fourth register.

8. The semiconductor integrated circuit according to claim 5, wherein

said voltage generating circuit further includes a fuse circuit of which setting can be varied in a non-volatile manner, and

said reference voltage generating circuit regulates said reference voltage in accordance with the setting of said fuse circuit.

9. The semiconductor integrated circuit according to claim 5, wherein

said voltage generating circuit further includes a fuse circuit of which setting can be varied in a non-volatile manner, and

said voltage conversion circuit adjusts drivability to drive a node outputting said internal power supply voltage in accordance with the setting of said fuse circuit.

10. The semiconductor integrated circuit according to claim 5, wherein

said operation circuit is a central processing unit (CPU) performing an operation in accordance with an instruction string, and

said semiconductor integrated circuit further includes a non-volatile memory circuit storing said instruction string.

11. The semiconductor integrated circuit according to claim 10, wherein

said voltage generating circuit further includes a fourth register holding a regulation value for generated said internal voltage,

said non-volatile memory circuit further holds an initial value of said regulation value, and

said central processing unit rewrites a value held in said fourth register in accordance with the value held in said third register.

12. The semiconductor integrated circuit according to claim 10, further comprising an input terminal for setting for mode switching, wherein

said central processing unit has a normal mode and a special mode as operation modes, in which special mode, a difference between said first and second digital values held in said first and second registers respectively is output as a third digital value, and said central processing unit makes a transition to said special mode in accordance with the setting of said input terminal at power-on.

13. The semiconductor integrated circuit according to claim 5, wherein

said operation circuit is a central processing unit performing an operation in accordance with an instruction string, and

said semiconductor integrated circuit further includes

a non-volatile memory circuit storing said instruction string and prescribed information, and

a volatile memory which is connected to said central processing unit and to

which said prescribed information is loaded from said non-volatile memory circuit by a boot program which is a part of said instruction string.

14. The semiconductor integrated circuit according to claim 5, wherein

said voltage conversion circuit has, as operation modes, a normal mode in which said external power supply voltage is lowered and a special mode in which said external power supply voltage is output without being converted, and

in said special mode, said first digital value corresponds to said external power supply voltage and is output from said second terminal.

15. The semiconductor integrated circuit according to claim 5, wherein

said internal circuit further includes

a fourth register holding an upper limit value of said internal power supply voltage, and

a fifth register holding a lower limit value of said internal power supply voltage, and

said operation circuit outputs an abnormal flag when the value held in said first register is not in a range between said upper limit value and said lower limit value.

16. The semiconductor integrated circuit according to claim 15, wherein

said operation circuit is a central processing unit performing an operation in accordance with an instruction string, and

said semiconductor integrated circuit further includes a non-volatile memory circuit storing said instruction string.

17. The semiconductor integrated circuit according to claim 15, wherein

said operation circuit is a central processing unit performing an operation in accordance with an instruction string, and

said semiconductor integrated circuit includes

a non-volatile memory circuit storing said instruction string and prescribed information, and

a volatile memory which is connected to said central processing unit and to which said prescribed information is loaded from said non-volatile memory circuit by a boot program which is a part of said instruction string.